

Mask Layout Fundamentals with Cadence Virtuoso

Physical layout, rule checking and advanced-packaging awareness

FA-0673 · 5 days

Embedded Systems and Hardware

Introduction

A five-day practical introduction to IC physical-layout workflows in Cadence Virtuoso for participants with semiconductor and CMOS knowledge. Develop selected device/layout examples, apply technology rules and examine connectivity and verification results.

The final day introduces advanced-packaging and Intel EMIB context. Practice uses the arranged tool, licences and teaching PDK; this is not a production tape-out, complete packaging implementation or qualification in mask fabrication.

Learning outcomes

- Navigate a prepared Virtuoso environment and its libraries/cell views.
- Explain how layout layers and technology rules relate to fabrication.
- Create and edit a small layout using the available rule-driven aids.
- Interpret introductory DRC, LVS and extraction concepts.
- Describe the role of bridge layout and separate package/analysis/signoff tools in an illustrative advanced-packaging flow.

Prerequisites

- Deep understanding of semiconductor devices and VLSI fundamentals.
- Experience with CMOS process concepts.

- Exposure to CAD/EDA tools (no deep Virtuoso experience required).
- Access to Cadence Virtuoso environment (with appropriate technology files).

Use the arranged teaching PDK and tool release; advanced rule decks and packaging integrations are demonstrations only where available.

Training outline

1. Day 1 — Layout Foundations and the Cadence Environment

Introduction to Mask Design

- How layout/mask layers relate to a fabrication process
- Role of mask design in IC fabrication flow.

Getting Started with Cadence Virtuoso

- Starting the environment and workspace basics.
- Overview of the layout editor vs. schematic views.
- Technology file and PDK basics.

Library and Cell Structure

- Library manager navigation.
- Creating a new layout cell.

2. Day 2 — Layout Creation and Editing

Layout Primitives

- Drawing rectangles, polygons, paths, and wires.
- Layer selection and visualization.

Basic Editing Techniques

- Move, resize, stretch, and property edits.
- Snap patterns and grid setup for correct alignment.

Manual Layout Example

- Simple device (e.g., transistor) layout.
- Understanding masks for each layer.

3. Day 3 — Technology Rules and Rule-driven Practice

Design Rule Concepts

- What design rules are and why they matter.

- Mapping rules to mask constraints.

DRD Editing in Virtuoso

- Design-Rule Driven editing fundamentals.

Track-Based and Snap-Pattern Techniques

- Introduction to width spacing patterns (WSPs) and snap patterns.

Hands-on Practice

- Applying the rules to layout test patterns.

Rule-driven editing reduces selected errors but does not establish complete correctness; checks depend on the PDK, configured rules and tool support.

4. Day 4 – Routing, Connectivity and Verification

Routing Techniques in Virtuoso

- Interactive and assisted routing.
- Selected point-to-point and differential-routing concepts where supported

Connectivity & Checks

- DRC concepts and running rule checks within Virtuoso.
- Layout vs schematic consistency checks (LVS overview).

Introduction to Parasitic Extraction and Checks

- Concept of extraction views and their relevance.

Run selected checks on the teaching example, distinguish geometry checks from circuit equivalence, and record issues rather than treating a passed basic exercise as signoff.

5. Day 5 – Advanced-packaging Context and Review

Overview of Advanced Packaging Flows

- What EMIB is and how it relates to mask design.
- Interaction between multi-die interconnect and layout/mask planning.

Virtuoso bridge-layout role in an illustrative EMIB flow

- Bridge signal, power and ground routing; distinguish this from separate package placement/routing tools
- High-level signal/power and layer-planning considerations

Integration with Other Tools

- Distinguish Pegasus physical-verification/signoff checks from Sigrity signal/power-integrity analysis; tool access and flows are setup-dependent

Review & Wrap-Up

- Summary of key learnings.

- Tips to continue self-study and real project practice.

Review an illustrative EMIB tool flow: Virtuoso bridge routing, separate package design, system planning, electrical/thermal analysis and signoff checks. No access to a proprietary production PDK or complete foundry-qualified flow is implied.