

Advanced IC Package Design with Siemens Xpedition

Substrate layout, constraints, verification and design handoff

FA-0662 · 5 days

Embedded Systems and Hardware

Introduction

A practical course for engineers with prior electronic-design experience, covering package and substrate design using Siemens EDA Xpedition Package Designer. A prepared design progresses through setup, floorplanning, placement, routing, checking and output review.

The five-day course uses selected advanced package examples. Available functions and integrations depend on the installed release, licences, technology files and lab setup; training exercises are not production signoff.

Learning outcomes

- Configure a prepared package-design project and its libraries and constraints.
- Develop and review substrate and multi-die floorplanning examples.
- Apply placement, routing, padstack and reuse techniques in a selected design.
- Interpret design checks and prepare supported handoff outputs for review.
- Consult release documentation when evaluating version-specific capabilities.

Prerequisites

- PCB or IC packaging knowledge and prior EDA tool experience.
- Familiarity with schematic/layout workflows and electronic-design data.
- Access to the arranged Xpedition installation, licences, technology files and lab workstation.

Training outline

1. Day 1 — Tool Setup and Design Preparation

Environment and Package Concepts

Xpedition Package Designer Interface

- Navigation, menus, toolbars, panels
- Workspace customization

Overview of IC Packaging Capabilities

- 2.5D/3D package support
- Substrate and interposer concepts

Installed-release capabilities and documentation

- Review interface and workflow differences in the arranged installation
- Identify supported package-design features and required licences
- Review documented pad-entry and physical-reuse controls where available

Projects, Constraints and Libraries

Project Setup

- Creating new package projects
- Template and technology files

Constraint Management

- Defining design rules and constraints
- Importing constraint sets

Library Setup

- Padstacks
- Cells and materials
- Part definition and pin mapping

2. Day 2 — Substrate and Die Floorplanning

2.5D/3D Stack Configurations

- Multi-die placement
- Die orientation and stacking methods

Platform Floorplanning Tools

- Integrated placement optimization
- Cross-domain design considerations

Placement and Physical Reuse

Placement Techniques

- Manual and assisted placement
- Group and block placement

Physical Reuse & Grouping

- Physical reuse elements
- Equivalency and replacement rules

3. Day 3 – Routing and Advanced Layout

Routing Fundamentals

- Sketch routing vs. automatic routing
- Differential pair routing

Complex Via Structures

- Microvia stacking and breakout strategies

Layer Stackup

- Defining and editing stackups
- Layer mapping between sources and targets

High-Speed & Signal Integrity Considerations

- Clock/data group rules
- Impedance control strategies

Compare routing and stackup choices in the prepared design; signal-integrity performance must be analysed with appropriate models and tools rather than inferred from a completed layout.

4. Day 4 – Verification, Integration and Data Management

In-design rule checking and connectivity verification

- On-the-fly rule checking

Geometry-Based DRC Essentials

- Writing and using custom rule sets
- Constraint Verification Approaches

7. Design Integration & Data Management

EDM Collaboration Workflows

- Database management and versioning

Forward/Back Annotation

- Integrating schematic and layout data
- Team-based Concurrent Design

Distinguish interactive design checks, connectivity verification and qualified signoff flows. Use only available tool integrations and technology-specific rules; a passed training DRC is not evidence that a package is manufacturing-ready.

5. Day 5 — Handoff and Integrated Design Review

Manufacturing Outputs

- Supported manufacturing and exchange outputs; compare Gerber, ODB++ and IPC-2581 where applicable
- 3D Model Export & Validation
- Package to PCB Integration Outputs

9. Practical Lab Sessions

Prepared package-design exercise

- Step-by-step substrate design
- Constraint-driven implementation
- Troubleshooting & Optimization Labs

10. Wrap-up & Next Steps

- Design Review Best Practices
- Common Pitfalls & Solutions
- Resources for Continued Learning (Mentor/Siemens EDA community)

Generate only export formats supported by the selected package workflow and review them against the receiving team's requirements. Complete a bounded substrate-design exercise and record unresolved rule, data or analysis issues.